IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A memory cell, comprising:

a vertical access device including a selective epitaxy mesa, wherein the selective epitaxy mesa comprises a portion of a buried conductive path, and wherein a region of the selective epitaxy mesa adjacent to the buried conductive path includes a laterally non-graded dopant profile consisting essentially of dopant of one conductivity type; and

a storage device on the selective epitaxy mesa.

2. (Original) The memory cell of claim 1, wherein selective epitaxy mesa includes a bottom source/drain and a top source/drain, and wherein the selective epitaxy mesa further includes a conductive body separating the bottom source/drain from the top source/drain.

3. (Original) The memory cell of claim 2, wherein the bottom source/drain is an in situ doped region.

4. (Original) The memory cell of claim 2, wherein the top source/drain is an in situ doped region.

5. (Original) The memory cell of claim 2, wherein the bottom source/drain includes a semi-annular ring around a bottom portion of the selective epitaxy mesa.

6. (Original) The memory cell of claim 5, wherein the vertical access device includes a signal line having a first height, and wherein the bottom source/drain includes a second height that is about equal to the first height.

7. (Original) The memory cell of claim 5, wherein the bottom source/drain is formed by out diffusion from an adjacent conductor.

8. (Original) The memory cell of claim 1, wherein the access device is free from a shallow trench isolation layer.

9. (Currently Amended) A vertical memory cell, comprising:

a substrate;

an access device including a selective epitaxy mesa formed on and extending outwardly from the substrate, wherein the selective epitaxy mesa comprises a portion of a buried conductive path, and wherein a region of the selective epitaxy mesa adjacent to the buried conductive path includes a laterally non-graded dopant profile consisting essentially of dopant of one conductivity type; and

a storage device on the selective epitaxy mesa.

10. (Original) The memory cell of claim 9, wherein the substrate includes silicon, and wherein the selective epitaxy mesa includes silicon.

11. (Currently Amended) The memory cell of claim 9, wherein the access device includes a body, a first source/drain region, a gate and a second source/drain region, wherein the body extends between the first source/drain region and the second source/drain region, and wherein the first source/drain region and the second source/drain region are each a selective epitaxy doped region of the selective epitaxy mesa.

12. (Original) The memory cell of claim 11, wherein the first source/drain region extends horizontally around the selective epitaxy mesa.

13. (Original) The memory cell of claim 12, wherein the first source/drain region is adapted to contact a bit line.

14. (Original) The memory cell of claim 12, wherein the second source/drain region is spaced from the substrate by the body.

15. (Original) The memory cell of claim 14, wherein the second source/drain region is an in situ N+ doped region of the selective epitaxy mesa.

16. (Currently Amended) A vertical memory cell, comprising:

a substrate;

an electrical signal line on the substrate;

an access device including:

a selective epitaxy mesa formed on and extending outwardly from the substrate, the selective epitaxy mesa including a first source/drain region adjacent the substrate and in electrical ~~electrically~~ communication with the electrical signal line, wherein a portion of the selective epitaxy mesa comprises a conductive portion of the electrical signal line, and wherein a region of the selective epitaxy mesa adjacent to the electrical signal line includes a lateral non-graded dopant profile consisting essentially of dopant atoms of one conductivity type; and

a storage device on the selective epitaxy mesa.

17. (Original) The vertical memory cell of claim 16, wherein the electrical signal line has a first height, and wherein the first source/drain region has a second height equal to or less than the first height.

18. (Original) The vertical memory cell of claim 16, wherein the selective epitaxy mesa cantilevers upwardly from the substrate, and wherein the selective epitaxy mesa includes an end, remote from the substrate, forming a second source/drain region.

19. (Original) The vertical memory cell of claim 16, wherein the first source/drain region extends around an outer periphery of the selective epitaxy mesa.

20. (Original) The vertical memory cell of claim 19, wherein the electrical signal line extends around the first source/drain region.

21. (Original) The vertical memory cell of claim 16, wherein the first source/drain region extends partially around an outer periphery of the selective epitaxy mesa.

22. (Original) The vertical memory cell of claim 21, wherein the electrical signal line extends around the first source/drain region.

23. (Original) The vertical memory cell of claim 21, wherein the electrical signal line partially around the selective epitaxy mesa.

24. (Original) The vertical memory cell of claim 16, wherein the first source/drain region is adapted to electrically communicate with a column address decoder through a buried bit line.

25. (Original) The vertical memory cell of claim 24, wherein the second source/drain region is adapted to electrically communicate with the storage device.

26. (Currently Amended) A vertical memory cell, comprising:

a substrate;

an electrical signal line on the substrate;

an access device including a selective epitaxy mesa formed on and extending outwardly from the substrate, the selective epitaxy mesa including a first source/drain region adjacent the substrate and in electrical ~~electrically~~ communication with the electrical signal line, wherein a portion of the selective epitaxy mesa comprises a conductive portion of the electrical signal line, and wherein a region of the selective epitaxy mesa adjacent to the electrical signal line includes a laterally non-graded dopant profile consisting essentially of dopant of one conductivity type, the selective epitaxy mesa further including a body extending vertically from the first source/drain region, an insulator on the body, and a gate on the insulator; and

a storage device on the selective epitaxy mesa remote from the substrate.

27. (Original) The vertical memory cell of claim 26, wherein the insulator surrounds the body, and wherein the gate surrounds the insulator such that the gate effects electrical conductivity of the body from more than one angle.

28. (Original) The vertical memory cell of claim 26, wherein the insulator surrounds the body, and wherein the gate partially overlies the insulator such that the gate effects electrical conductivity of the body from more than one angle.

29. (Original) The vertical memory cell of claim 28, wherein the gate overlies over half of a surface area of the body.

30. (Original) The vertical memory cell of claim 26, wherein the electrical signal line includes titanium.

31. (Currently Amended) A vertical transistor, comprising:

a vertical, selective epitaxy body extending from a horizontal substrate such that a portion of the selective epitaxy body is adapted to comprise a vertical portion of a buried bit line, wherein a region of the selective epitaxy body adjacent to the vertical portion includes a laterally non-graded dopant profile consisting essentially of dopant of one conductivity type;

a first doped region in the body adjacent the substrate;

a second doped region in the body remote from the substrate;

an undoped intermediate region between the first doped region and the second doped region; and

a gate at least partially surrounding the intermediate region.

32. (Original) The transistor of claim 31, wherein the body is adapted to form a channel between the doped first region and the doped second region.

33. (Currently Amended) The transistor of claim 31, wherein the first doped region is adapted to be in electrically communication with [a] the buried bit line.

34. (Original) The transistor of claim 31, wherein the gate is adapted to be in electrical communication with a word line.

35. (Original) The transistor of claim 31, wherein the gate overlies at least half of the surface area of the intermediate region.

36. (Original) The transistor of claim 31, wherein the gate overlies at least about 75% of the surface area of the intermediate region.

37. (Original) The transistor of claim 31, wherein the gate overlies about all of the surface area of the intermediate region.

38. (Original) The transistor of claim 31, wherein the vertical, selective epitaxy body is generally cylindrical.

39. (Original) The transistor of claim 38, wherein the gate is generally annular and extends completely around the body.

40. (Original) The transistor of claim 38, wherein the first doped region is cylindrical.

41-70. (Canceled)

71. (New) The memory cell of claim 1, wherein the selective epitaxy mesa includes a region of polycrystalline silicon.

72. (New) The memory cell of claim 1, wherein the region of the selective epitaxy mesa adjacent to the buried conductive path comprises at least one abrupt p-n junction.

73. (New) The memory cell of claim 1, wherein the region of the selective epitaxy mesa adjacent to the buried conductive path comprises at least one abruptly doped region.